**Project: AM62A32AOMHIAMBR SoM Design Overview**

**1. Processor**: Texas Instruments AM62A32AOMHIAMBR

* Dual-core Arm Cortex-A53 (up to 1.4 GHz)
* Single Cortex-R5F core for real-time control
* C7x DSP with MMA for vision and AI (up to 1 TOPS)
* Integrated ISP for MIPI CSI-2 camera
* 24-bit RGB parallel display interface

**Memory**:

* LPDDR4, 32-bit bus, inline ECC
* Target speed: up to 3733 MT/s
* Layout per TI's high-speed routing guidelines

**Camera Interface**:

* MIPI CSI-2 receiver
* 4-lane D-PHY, up to 1.5 Gbps per lane
* CSI termination and lane matching required

**Display Interface**:

* 24-bit RGB parallel output (DPI)
* Supports up to 2048x1080 @ 60Hz
* Independent pixel clock (up to 165 MHz)

**Power Architecture**:

* PMIC selection TBD based on power rails:
  + 0.85V core
  + 1.1V PLL
  + 1.5V/1.8V I/O
  + 3.3V peripherals
* Power sequencing and supervision required

**Board Design Goals**:

* KiCad-based schematic and layout
* Support for camera module and RGB display
* Small form factor SoM module
* Breakout baseboard for development